DATE: 9/22/80

CLASSIFICATION

2200 SYSTEMS

CATEGORY

INTERFACE

PRODUCT/APPL.

I/O CONTROLLERS

SEQUENCE

5

TITLE:

MODEL 22C80 DISK MULTIPLEXER INTERFACE CONTROLLER (WL# 177-2280C)

This PSN contains the following 2280 Disk Multiplexer Interface Controller information.

1. GENERAL DESCRIPTION
2. SWITCH SETTINGS
3. INSTALLATION
4. SYSTEM INTERCONNECTION
5. DIAGNOSTICS
6. TROUBLESHOOTING
7. HARDWARE THEORY OF OPERATION (MAJOR-FUNCTION LEVEL)

Following is a list of documentation categories referenced by this PSN. Documentation from these other categories is required for the performance of certain installation/maintenance tasks.

Device Address Switch Settings -- IV.B.1-3
CPU Power Supply Voltage Adjustments -- IV.A.3
2280MUX System Interconnection -- IV.B.3
2280 Disk Diagnostic -- IV.C.1
1. GENERAL DESCRIPTION

The Model 22C80 I/O controller (WL# 177-2280C or WL# 210-7715) provides the input/output interface between a 2200VP/LVP/MVP Central Processing Unit and a 2280 Disk Multiplexer (2280MUX).

2. SWITCH SETTINGS

See FIGURE 1 for information concerning the setting of device address switch SW1. The device addresses normally used for the 2280 Disk Drive are HEX 10 (primary address), HEX 20 (secondary address), or HEX 30 (secondary address). Refer to PSN IV.B.1-3 for more information concerning the setting of device address switches.

NOTE:

The HEX values given in FIGURE 1 are correct only for boards at Revision 2 and above. For R0 and R1 boards (limited distribution) the HEX values are as follows.

<table>
<thead>
<tr>
<th>SWITCH #</th>
<th>HEX VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>01</td>
</tr>
<tr>
<td>2</td>
<td>80</td>
</tr>
<tr>
<td>3</td>
<td>20</td>
</tr>
<tr>
<td>4</td>
<td>10</td>
</tr>
<tr>
<td>5</td>
<td>08</td>
</tr>
<tr>
<td>6</td>
<td>04</td>
</tr>
<tr>
<td>7</td>
<td>02</td>
</tr>
<tr>
<td>8</td>
<td>NOT USED</td>
</tr>
</tbody>
</table>

3. INSTALLATION

The 22C80 can be installed in any available I/O slot in the 2200VP/LVP/MVP CPU. Be certain to power-off the CPU before installing the controller. Prior to inserting the 22C80 in a CPU, ensure that all switches on that board are set correctly (ref: Section 2). Also check to see that the fingerboard connectors are clean.

After installing the 22C80 in a unit, be certain to recheck and adjust, if necessary, CPU power supply voltages +5V (I/O) and -12V. Refer to documentation category IV.A.3 for the appropriate CPU voltage adjustment procedures.
FIGURE 1 WL NO. 210-7715 22C80 INTERFACE BOARD
4. SYSTEM INTERCONNECTION

The I/O cables (WL# 220-0138) attached to jacks J1-J3 on the 2280MUX Multiplexer board (WL# 210-7717), and to jacks J1-J4 on the 2280MUX Port Expander boards (WL# 210-7718) connect to the 22C80 controller in each CPU of the multiplex system (see "Star" configuration below). Refer to documentation category IV.B.3 for more information concerning 2280MUX system interconnection.
5. DIAGNOSTICS

Up to the date of this publication, diagnostics designed to test all 2280MUX functions, as well as the associated 22C80 controllers, had not been completed. It is possible to test a majority of the 2280MUX and 22C80 functions with the standard 2280 Disk Diagnostic (WL# 701-2555). This is accomplished by running the diagnostic at several (a predetermined number) CPU's at the same time, with each CPU addressing a different disk surface (one surface only) in the drive. The predetermined number of CPU's at which the diagnostic can be run is equal to the number of data surfaces present in the drive under test (that is, 2280-1: two surfaces; 2280-2: four surfaces; 2280-3: six surfaces). Refer to documentation category IV.C.1 for detailed information concerning the standard 2280 Disk Diagnostic.

6. TROUBLESHOOTING

If only one channel of a 2280MUX system fails (I/O error indication), it is possible to isolate the cause of the failure by interchanging the I/O cables at the Port Expander board or Multiplexer board (as applicable) in the 2280 DPU/MUX. If, after swapping CPU-to-MUX cables, the problem remains with the same 2280MUX channel, conclude that the Port Expander/Multiplexer is defective; if the problem moves with the suspected 2200 CPU to the different 2280MUX channel, conclude that the 2200 CPU is defective—the most likely cause being the 22C80 I/O controller. If all channels fail, the 2280 DPU, the DPU/MUX power supply, the 2280MUX multiplexer board, the disk cables, or the 2280 disk itself may be defective.

7. HARDWARE THEORY OF OPERATION (MAJOR-FUNCTION LEVEL)

Address Bus and Control Circuitry (ref: FIGURE 2 and MNEMONICS)

Device Address Switch--

Represents the device address of the 2280 Disk Drive. This address is chosen by the customer and set by the Customer Engineer. The outputs of the switch are inputs to the Address Compare Circuit.
Address Compare Circuit--

Verifies the device address received from the CPU via the Address Bus (AB1-AB8) against the address represented by the Device Address Switch. The output of the compare circuit is input to the Select Latch. The output also enables operation of the DN3 Latch.

Select Latch--

Produces a Select (SEL) signal if the device address received from the CPU and the address represented by the Device Address Switch setting are identical. This Select signal in turn generates a Request (REQ) signal, which is sent to the 2280 Disk Multiplexer (2280MUX) indicating the CPU requires disk access. The Select signal also enables operation of the Control Decoder, and the OBS Latch.

DN3 Latch--

Monitors CPU Address Bus bit 7 (HEX 40) to determine whether access to the second 2280 Disk Drive in a daisy-chain configuration is requested. If the second drive is specified, a DN3 signal is sent to the 2280MUX indicating such.

Control Decoder--

Decodes control data received from the CPU via the Output Bus (OB1, and OB8) into the desired command as follows:

<table>
<thead>
<tr>
<th>COMMAND</th>
<th>LOGIC LEVEL</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>&quot;0&quot;</td>
</tr>
<tr>
<td>OB1 Clear</td>
<td>OB8 Parity</td>
</tr>
<tr>
<td></td>
<td>Error</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Hog Latch--

When a "Hog" command is decoded (see Control Decoder), the Hog Latch produces a Request (REQ) signal which is sent to the 2280MUX indicating the CPU requires exclusive use of the disk.
When a "Release Disk" command is decoded, the Hog Latch terminates the Request signal.

Disk Ready/Busy Circuit--

Monitors the Ready/Busy signal received from the disk (DRBY), and relays that status to the CPU.

OBS Latch--

Generates an Output Data Strobe (ODS) which strobes the Output Data to the 2280MUX.

Shift Register--

Produces the timing pulses required for controlling the transfer of data between the CPU and the 2280MUX.

Level Converters (Line Receivers/Drivers)--

Convert TTL voltage levels to the differential voltage levels (Emitter Coupled Logic--ECL--levels) required by the 2280MUX Port Expander board. Use of ECL in this application allows each CPU disk I/O logic to operate at optimum speed even with the greater distance from CPU to multiplexer, as compared to the driver/receiver distances possible with TTL.
Input Bus Circuitry (ref: FIGURE 3 and MNEMONICS)

Input Data Demultiplex Latches (Data)--

Receives the read data that is to be sent to the CPU from the 2280MUX Port Expander board. On the leading edge of the Input Data Strobe (IDS), the low order Input Data bits (ID1-ID4) are selected through the demultiplexer, and are then sent to the Parity Checker and the Input Bus Mux. On the trailing edge of IDS, the high order bits (ID5-ID8) are selected through the demultiplexer.

Input Data Demultiplex Latches (Disk Status)--

Receives the disk status from the 2280MUX Port Expander board. On the leading edge of the Status Request Strobe (SRB), the low order Input Data bits (ID1-ID4) are selected through the demultiplexer as S1-S4, and are sent to the Input Bus Mux for transmission to the CPU. On the trailing edge of SRB, the high order bits (ID5-ID8) are selected through the demultiplexer as S5-S8.

Input Bus Mux--

Selects either disk status or data as Input Bus bits I81-I88, and transmits the information to the CPU.

Parity Checker--

Verifies the parity bit, which is received along with the Input Data for integrity. If the parity bit is incorrect the Parity Error Latch is set.

Parity Error Latch--

Indicates a parity error occurring during transfer of data between the 2280MUX and the 22C80 Interface.
Level Converters (Line Receivers/Drivers)--

Convert differential voltage levels (Emitter Coupled Logic--ECL--levels) received from the 2280MUX Port Expander board to the TTL levels required by the 22C80 Interface board. Use of ECL in this application allows each CPU disk I/O logic to operate at optimum speed even with the greater distance from CPU to multiplexer, as compared to the driver/receiver distances possible with TTL.
Output Bus Circuitry  (ref: FIGURE 4 and MNEMONICS)

Output Bus Mux--

Receives the write data that is to be sent to the disk from the CPU Output Bus (OB1-OB8). During the first half of the Output Bus Strobe (OB5), the low order bits (OB1-OB4) are selected through the Output Bus Mux as Output Data bits OD1-OD4. During the second half of the OB5, the high order bits (OB5-OB8) are selected through the multiplexer. The Output Data bits are sent to the 2280MUX for transmission to the disk drive.

Parity Generator--

Accepts the write data that is to be sent to the disk from the CPU Output Bus (OB1-OB8), and generates a parity bit (OD5) which is sent to the 2280MUX along with the Output Data.

Level Converters (Line Receivers/Drivers)--

Convert TTL voltage levels to the differential voltage levels (Emitter Coupled Logic--ECL--levels) required by the 2280MUX Port Expander board. Use of ECL in this application allows each CPU disk I/O logic to operate at optimum speed even with the greater distance from CPU to multiplexer, as compared to the driver/receiver distances possible with TTL.
**SIGNAL MNEMONICS**

**AB1-AB8 (Address Bus):**
Address data for I/O controller selection -- from CPU

**AB7 (Address Bus):**
Indicates access to second drive is required -- from CPU

**ABS (Address Bus Strobe):**
Strobes address data to I/O controller

**ACK (Acknowledge):**
Acknowledgement of CPU request for disk use -- from Port Expander (210-7718)

**ACK (Acknowledge):**
Acknowledgement of CPU request for disk use -- internal

**BK1:**
Clears Parity Error Latch -- internal

**BK3:**
Selects either low or high order data as Output Data -- internal

**CBS (Control Bus Strobe):**
Strobes control data to I/O controller -- from CPU

**CLKB (Clock B):**
Selects AB6 as OD5 -- internal

**CPB (Central Processor Busy):**
CPU ready/busy status -- from CPU

**CPB (Central Processor Busy):**
CPU ready/busy status -- internal

**DN3 (Disk Number 3):**
Indicates access to second drive is required -- internal

**DRB (Disk Ready/Busy):**
Disk ready/busy status -- from Port Expander (210-7718)
DRB (Disk Ready/Busy):
Disk ready/busy status -- internal

DRBY (Disk Ready/Busy):
Disk ready/busy status -- internal

HOG:
Initiates exclusive use of disk -- internal

IB1-IB8 (Input Bus):
Read data to be sent to CPU -- to CPU

IB9 (Input Bus):
ENDI bit -- to CPU

IBS (Input Bus Strobe):
Strobes write data from disk to CPU -- to CPU

ID1-ID5 (Input Data):
Read data to be sent to CPU -- from Port Expander (210-7718)

ID1-ID4 (Input Data):
Status to be sent to CPU -- internal

ID1-ID5 (Input Data):
Read data to be sent to CPU -- internal

ID5 (Input Data):
Generates ENDI bit -- internal

IDS (Input Data Strobe):
Strobes read data from disk to CPU -- from Port Expander (210-7718)

IDS (Input Data Strobe):
Strobes read data from disk to CPU -- internal

OB1-OB8 (Output Bus):
Write data to be sent to disk -- from CPU

OB1 (Output Bus):
Decoded into control signals -- from CPU
OB8 (Output Bus):
Decoded into control signals -- from CPU

OB3 (Output Bus Strobe):
Strobes write data from CPU to disk -- from CPU

OD1-OD4 (Output Data):
Write data to be sent to disk -- internal

OD5 (Output Data):
Parity bit for write data to be sent to disk -- internal

OD1-OD5 (Output Data):
Write data to be sent to disk -- to Port Expander (210-7718)

OD8 (Output Data Strobe):
Strobes write data from CPU to disk -- internal

OD8 (Output Data Strobe):
Strobes write data from CPU to disk -- to Port Expander (210-7718)

PE (Parity Error):
Parity error indication -- internal

PRMS (Prime Signal):
Resets DPU and disk -- from CPU

R/B (Ready/Busy):
Disk ready/busy status -- to CPU

REQ (Request):
Request by CPU for disk use -- internal

REQ (Request):
Request by CPU for disk use -- to Port Expander (210-7718)

RESET:
Resets DPU and disk -- internal

RESET:
Resets DPU and disk -- to Port Expander (210-7718)
$S_1$-$S_7$ (Status):
Status to be sent to CPU -- internal

$S_8$ (Status):
Determines disk ready/busy status -- internal

SEL (Selected):
Indicates I/O controller selected -- internal

SRB (Status Request Bit):
Strobes disk status to the 22C80 -- from Port Expander (210-7718)

SRB (Status Request Bit):
Strobes disk status to the 22C80 -- internal

UNHOG:
Terminates exclusive use of disk -- internal