This PSN contains the following 2280 Disk Multiplexer information.

1. GENERAL DESCRIPTION
2. PHYSICAL CHARACTERISTICS
3. INSTALLATION
4. DIAGNOSTICS
5. TROUBLESHOOTING
6. HARDWARE THEORY OF OPERATION (MAJOR-FUNCTION LEVEL)

Following is a list of documentation categories referenced by this PSN. Documentation from these other categories is required for the performance of certain installation/maintenance tasks.

22C80 Disk Multiplexer Interface -- IV.B.1
2280 DPU-to-2280 DPU/MUX Conversion -- I.B.2
2280 DPU Power Supply Voltage Adjustments -- III.A.7
2280 Disk Diagnostic -- IV.C.1
1. GENERAL DESCRIPTION

The Model 2280 Disk Multiplexer (hereinafter referred to as the 2280MUX) is optionally resident in the 2280 Disk Processing Unit (DPU) and permits two to fifteen 2200VP/LVP/MVP Central Processing Units to share one or two Model 2280 Disk Drives (Phoenix Drive or CDC 9448 Cartridge Module Drive--CMD). Unlike earlier disk multiplexers, which were of the "daisy-chain" type, the 2280MUX is a "star" type multiplexer. In a "star" configuration, the CPU's are individually connected directly to the multiplexer. (See FIGURE 1.)

The 2280MUX allocates disk time to multiple systems in a manner that enables all systems to have virtually concurrent access to the disk. The multiplexer sequentially polls all systems until one of the systems attempts to access the disk. At that point, the multiplexer momentarily ceases polling and passes control of the disk to the inquiring system, which is permitted to execute a single disk statement or command. The multiplexer does not monitor the amount of time required to execute each statement, nor does it limit the number of sectors transferred by a statement. A single statement may read or write only one sector, or may carry out multi-sector transfers. (For example, a MOVE or COPY statement might transfer the contents of an entire disk platter to a second platter; however, major file maintenance operations should be executed only by a system in Hog Mode--see following). When execution of the single disk operation is completed, sequential polling of on-line CPU's resumes from the last requesting CPU.

Some disk operations, such as the on-line updating of a shared common file, require that one system have a period of exclusive, uninterrupted access to the disk. For such operations, the $OPEN statement from the Wang BASIC-2 language should be used (ref: 2200VP BASIC-2 Language Reference Manual, WL# 700-4080, IV.C.2). In this mode of operation, one system temporarily monopolizes or "hogs" the disk, locking out all other systems. Critical file maintenance operations may then be carried out by the privileged system without interruption. After file maintenance has been completed, the $CLOSE statement should be used to release the disk, restoring all CPU's to equal disk-access priority.
2. PHYSICAL CHARACTERISTICS

The 2280MUX consists of the following:

-- A Multiplexer board (WL# 177-2280-X or WL# 210-7717) containing the polling and port-selection circuitry, which interfaces the 2280 Disk Processing Unit (DPU) and up to three CPU's.

-- Up to three Port Expander boards (WL# 177-2280-XE or WL# 210-7718), each of which interfaces up to four additional CPU's.

The 2280MUX circuit boards install directly into a Model 2280 Disk Processing Unit. (A special DPU motherboard (WL# 210-7716) is required. More detailed information follows.)

Each CPU connected to the 2280MUX must have a Model 22C80 I/O controller (WL# 177-2280-C or WL# 210-7715) to interface the 2280MUX.

NOTE:

Refer to documentation category IV.B.1 for information concerning the required 22C80 I/O controller.

For system interconnection, standard 12-foot (3.6-meter) I/O cables (WL# 220-005-3) are supplied with the multiplexer. Extension cables are available, allowing for a maximum distance between CPU and 2280MUX of 1,012 ft (306.7 m). Extension cable lengths and part numbers are as follows:

<table>
<thead>
<tr>
<th>LENGTH (FEET)</th>
<th>LENGTH (METERS)</th>
<th>WL #</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>7.6</td>
<td>120-2280-01</td>
</tr>
<tr>
<td>50</td>
<td>15.2</td>
<td>120-2280-02</td>
</tr>
<tr>
<td>100</td>
<td>30.3</td>
<td>120-2280-03</td>
</tr>
<tr>
<td>250</td>
<td>75.8</td>
<td>120-2280-04</td>
</tr>
<tr>
<td>500</td>
<td>151.5</td>
<td>120-2280-05</td>
</tr>
<tr>
<td>750</td>
<td>227.3</td>
<td>120-2280-06</td>
</tr>
<tr>
<td>1000</td>
<td>303.0</td>
<td>120-2280-07</td>
</tr>
</tbody>
</table>

A 15-inch (37.5-cm) cable (WL# 220-0257) is also provided for connecting the Multiplexer board (WL# 210-7717) to the ALU/MUX board (WL# 210-7421-A) in the DPU.
FIGURE 1 below illustrates a typical four-system, dual-drive configuration. Two unused (not required) Port Expander boards are also shown in the figure.
3. INSTALLATION

NOTE:
Be sure to power-off the 2280 DPU/MUX before performing any installation procedure.

3.1 MOTHERBOARD REQUIREMENTS

The 2280MUX requires that a WL# 210-7716 motherboard be resident in the 2280 Disk Processing Unit (DPU). Model 2280 DPU's sold with the MUX have a WL# 210-7716 motherboard. All newly manufactured 2280 DPU's also have this motherboard installed, providing for easier installation of a MUX upgrade.

If an older-version 2280 DPU is to be upgraded to add multiplex capabilities, the entire 2280 DPU chassis must be replaced with the newer-version chassis (WL# 270-0688-60 for 60 Hz, or WL# 270-0688-50 for 50 Hz), containing a WL# 210-7716 motherboard.

Refer to documentation category I.B.2 for detailed conversion procedures, and then continue with Section 3.2 of this installation procedure.

3.2 MOTHERBOARD AC INPUT VOLTAGE SELECTION JUMPERS

Jumper wires are provided on the WL# 210-7716 motherboard for ac input voltage (115V or 230V) selection. Two jumpers are installed for 115VAC and one jumper for 230VAC. FIGURE 1 shows the positions of these jumpers. Be certain the jumper configuration is correct for the supplied ac voltage (see following chart).

<table>
<thead>
<tr>
<th>VOLTAGE SELECTION JUMPERS</th>
<th>115VAC</th>
<th>230VAC</th>
</tr>
</thead>
<tbody>
<tr>
<td>JUMPER A</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>JUMPER B</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>JUMPER C</td>
<td>OUT</td>
<td>IN</td>
</tr>
</tbody>
</table>

3.3 MOTHERBOARD/PCB LAYOUT

The locations of the 2280MUX circuit boards in relation to the motherboard/chassis are shown in FIGURE 1. Ensure that all fingerboard connectors are clean prior to installing the boards in the DPU. (An ink eraser should be used to clean the pins if necessary.)
After installing the 2280MUX circuit boards, be certain to recheck and adjust, if necessary, DPU power supply voltages +5V and -12V. Refer to Wang Cartridge Module Disk Drive Field Level Maintenance Manual Addendum One, CE #03-0080-A (III.A.7), for 2280 DPU voltage adjustment procedures.

3.4 SYSTEM INTERCONNECTION

Refer to FIGURES 1, 2, 3, and the following table when interconnecting CPU's and 2280MUX.

<table>
<thead>
<tr>
<th>TABLE 1 2280MUX SYSTEM CABLE CONNECTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CABLE #</td>
</tr>
<tr>
<td>220-0138</td>
</tr>
<tr>
<td>220-0138</td>
</tr>
<tr>
<td>220-0138</td>
</tr>
<tr>
<td>220-0138</td>
</tr>
<tr>
<td>220-0138</td>
</tr>
<tr>
<td>220-0138</td>
</tr>
<tr>
<td>220-0138</td>
</tr>
<tr>
<td>220-0138</td>
</tr>
<tr>
<td>220-0138</td>
</tr>
<tr>
<td>220-0257</td>
</tr>
</tbody>
</table>

4. DIAGNOSTICS

Up to the date of this publication, diagnostics designed to test all 2280MUX functions had not been completed. It is possible to test a majority of the 2280MUX functions with the standard 2280 Disk Diagnostic (WL# 701-2555). This is accomplished by running the diagnostic at several (a predetermined number) CPU's at the same time, with each CPU addressing a different disk surface (one surface only) in the drive. The predetermined number of CPU's at which the diagnostic can be run is equal to the number of data surfaces present in the drive under test (that is, 2280-1: two surfaces; 2280-2: four surfaces; 2280-3: six surfaces).

Refer to documentation category IV.C.1 for detailed information concerning the standard 2280 Disk Diagnostic.
FIGURE 2  WL NO. 210-7717 MULTIPLEXER BOARD
FIGURE 3 WL NO. 210-7718 PORT EXPANDER BOARD
5. TROUBLESHOOTING

If only one channel of a 2280MUX system fails (I/O error indication), it is possible to isolate the cause of the failure by interchanging the I/O cables at the Port Expander board or Multiplexer board (as applicable) in the 2280 DPU/MUX. If, after swapping CPU-to-MUX cables, the problem remains with the same 2280MUX channel, conclude that the Port Expander/Multiplexer is defective; if the problem moves with the suspected 2200 CPU to the different 2280MUX channel, conclude that the 2200 CPU is defective—the most likely cause being the 22C80 I/O controller.

If all channels fail, the 2280 DPU, the DPU/MUX power supply, the 2280MUX multiplexer board, the disk cables, or the 2280 disk itself may be defective.

6. HARDWARE THEORY OF OPERATION (MAJOR-FUNCTION LEVEL)

Port Expander Board (WL #210-7718) (ref: FIGURE 4 and MNEMONICS)

Port Selector--

Decodes the port-select signals (50–1), received from the Multiplexer board, into port-select signals P1–4. These signals enable one of four CPU I/O ports on the Port Expander board.

Reset Mux--

Selects the appropriate Reset pulse (RESET1–4), received from the CPU's, for output to the Multiplexer board as ICAPM. The Reset pulse is used to initialize the DPU, the MUX, and the disk drive.

Request Latch--

Selects the appropriate Request signal (REQ1–4), received from the CPU's, for output to the Multiplexer board as RQ1–4. The Request line informs the DPU that a CPU requires disk access.
Input Bus Mux--

Receives the read data (IB₁₋₈) that is to be sent to the CPU. During the first half of the Input Data Strobe (IDS), the low order bits (IB₁₋₄) are selected through the Input Bus Mux as Input Data bits ID₁-ID₄. During the second half of the IDS, the high order bits (IB₅₋₈) are selected through the multiplexer. The Input Data bits are sent to the CPU's, via the 22C80 I/O controller.

Level Converters (Line Receivers/Drivers)--

Convert differential voltage levels (Emitter Coupled Logic--ECL--levels) received from the CPU's (22C80) to the TTL levels required by the Multiplexer board. Convert TTL voltage levels received from the Multiplexer board to the differential driving levels required by the CPU's (22C80). Use of ECL in this application allows each CPU disk I/O logic to operate at optimum speed even with the greater distance from CPU to multiplexer, as compared to the driver/receiver distances possible with TTL.

PORT EXPANDER SIGNAL MNEMONICS

ACK₁₋₄ (Acknowledge):

Acknowledgement of CPU request for disk use -- from MUX (210-7717)

ACK (Acknowledge):

Acknowledgement of CPU request for disk use -- to CPU's (22C80)

CLK (Clock):

Clocks Request Latch -- from MUX (210-7717)

CPB (Central Processor Busy):

CPU ready/busy status -- from CPU's (22C80)

CPB (Central Processor Busy):

CPU ready/busy status -- to MUX (210-7717)
DN3 (Disk Number 3):
Indicates access to second drive is required -- from CPU's (22C80)

DN3 (Disk Number 3):
Indicates access to second drive is required -- to MUX (210-7717)

DOD1-DOD4 (Data Out to Disk):
Write data to be sent to disk -- to MUX (210-7717)

DRB (Disk Ready/Busy):
Disk ready/busy status -- to CPU's (22C80)

DS (Data Select):
Selects IB1-4 or IB5-8 for output -- from MUX (210-7717)

IB1-8 (Input Bus):
Read data to be sent to CPU's -- from MUX (210-7717)

ICAPM (Input Calculator Prime):
Resets DPU and disk -- to MUX (210-7717)

ID1-ID4 (Input Data):
Read data to be sent to CPU's -- to CPU's (22C80)

IDS (Input Data Strobe):
Strobes read data from disk to CPU's -- to CPU's (22C80)

I0B1 (Input/Output Bit 1):
Parity bit for write data to be sent to disk -- from CPU's (22C80)

I0B1 (Input/Output Bit 1):
Parity bit for write data to be sent to disk -- to MUX (210-7717)

OBS (Output Bus Strobe):
Strobes write data from CPU's to disk -- from CPU's (22C80)

OBS (Output Bus Strobe):
Strobes write data from CPU's to disk -- to MUX (210-7717)

OD1-OD4 (Output Data):
Write data to be sent to disk -- from CPU's (22C80)
P1-4 (Port):
    Select appropriate CPU port circuitry -- internal

RB (Ready/Busy):
    Disk ready/busy status -- from MUX (210-7717)

REQ1-4 (Request):
    Request by CPU for disk use -- from CPU's (22C80)

RESET1-4:
    Reset DPU and disk -- from CPU's (22C80)

RQ1-4 (Request):
    Request by CPU for disk use -- to MUX (210-7717)

S0-1 (Select):
    Decoded into port select signals -- from MUX (210-7717)

STR (Strobe):
    Strobes read data from disk to CPU's -- from MUX (210-7717)
*1 - ODI-OD4, IOB1, DN3, CPB, OBS  
*2 - DOD1-DOD4, IOB1, DN3, CPB, OBS  
*3 - RB, STR, ACK1-4  
*4 - DRB, IDS, ACK

**FIGURE 4 PORT EXPANDER BLOCK DIAGRAM**
Multiplexer Board (WL #210-7717) (ref: FIGURE 5 and MNEMONICS)

Output Data Latch--

Receives the write data (DOD1-DOD4) that is to be sent to (written on) the disk. During the first half of the Output Bus Strobe (OBS), the data-out bits are clocked through the Output Data Latch as KS0-KS3. During the second half of OBS, the data-out bits are clocked through the latch as KS4-KS7. The KS bits are sent to the disk via the DPU.

Reset Mux--

Selects the appropriate (desired) Reset pulse (RESET1-RESET3) received from the CPU's for output to the DPU as ICAPM. The Reset pulse is used to initialize the DPU and disk drive.

Request Latch--

Selects the appropriate (desired) Request signal (REQ1-REQ3) received from the CPU's. The Request line informs the DPU that a CPU requires disk access.

Polling Circuit--

Scans the CPU request lines (RQ1-RQ4) to determine whether disk access is desired. When a request is received, the multiplexer sends an acknowledge signal (ACK1-ACK4) to the requesting CPU, and the polling sequence is momentarily halted until that CPU completes its disk operation. Polling resumes with the next sequential channel. RESET initializes the polling circuit to a count of one (channel #1 of the WL# 210-7717 Multiplexer board).

Clock--

Increments the CPU polling circuit.

Decode Control Circuit--

Monitors the acknowledge signals (ACK1-ACK4), and decodes these signals
into the appropriate Board Select (BS1-BS4), Port Select (P1-P3), and Select (S0-S1) signals.

Port Selector--

Decodes the port-select signals (S0-S1) into port-select signals P1-P3. These signals enable the port circuitry for the CPU requiring disk access.

CPU Ready/Busy Latch--

Provides the DPU with the CPU ready/busy status.

Input Bus Strobe Latch--

Receives the Input Bus Strobe from the DPU, and retransmits the strobe to each CPU at the appropriate time.

Input Bus Mux--

Receives the read data (IB1-IB8) that is to be sent to the CPU. During the first half of the Input Bus Strobe (IBS), the low order bits (IB1-IB4) are selected through the Input Bus Mux as Input Data bits ID1-ID4. During the second half of the IBS, the high order bits (IB5-IB8) are selected through the multiplexer. The Input Data bits are sent to the CPU's via the 22C80 I/O controller.

Level Converters (Line Receivers/Drivers)--

Convert differential voltage levels (Emitter Coupled Logic--ECL--levels) received from the CPU's (22C80) to the TTL levels required by the Multiplexer board. Convert TTL voltage levels received from the Multiplexer board to the differential driving levels required by the CPU's (22C80). Use of ECL in this application allows each CPU disk I/O logic to operate at optimum speed even with the greater distance from CPU to multiplexer, as compared to the driver/receiver distances possible with TTL.
MULTIPLEXER SIGNAL MNEMONICS

ACK\textsubscript{1-3} (\textit{Acknowledge}):

Acknowledgement of CPU request for disk use -- internal

ACK\textsubscript{2-4} (\textit{Acknowledge}):

Acknowledgement of CPU request for disk use -- to Port Expanders (210-7718)

ACK (\textit{Acknowledge}):

Acknowledgement of CPU request for disk use -- to CPU's (22C80)

BS\textsubscript{2-BS4} (\textit{Board Select}):

Selects the appropriate Port Expander -- to Port Expanders (210-7718)

CLK (\textit{Clock}):

Clocks Request Latch -- internal

CPB (\textit{Central Processor Busy}):

CPU ready/busy status -- from CPU's (22C80)

CP\textsubscript{B} (\textit{Central Processor Busy}):

CPU ready/busy status -- to DPU (210-7421-A)

DN\textsubscript{3} (\textit{Disk Number 3}):

Indicates access to second drive is required -- from CPU's (22C80)

DN\textsubscript{3} (\textit{Disk Number 3}):

Indicates access to second drive is required -- to DPU (210-7421-A)

DOD\textsubscript{1-DOD4} (\textit{Data Out to Disk}):

Write data to be sent to disk -- internal

DRB (\textit{Disk Ready/Busy}):

Disk ready/busy status -- to CPU's (22C80)

DS (\textit{Data Select}):

Selects IB1-IB4 or IB5-IB8 for output -- internal

GIS\textsubscript{O}:

Strobes write data from CPU's to disk -- to DPU (210-7421-A)
GKBD:
  CPU ready/busy status -- to DPU (210-7421-A)

IBS (Input Bus Strobe):
  Strobes read data from disk to CPU's -- from DPU (210-7421-A)

IB1-IB8 (Input Bus):
  Read data to be sent to CPU's -- from DPU (210-7421-A)

ICAPM (Input Calculator Prime):
  Resets DPU and disk -- to DPU (210-7421-A)

ID1-ID4 (Input Data):
  Read data to be sent to CPU's -- to CPU's (22C80)

IDS (Input Data Strobe):
  Strobes read data from disk to CPU's -- to CPU's (22C80)

IOB1 (Input/Output Bit 1):
  Parity bit for write data to be sent to disk -- from CPU's (22C80)

IOB7 (Input/Output Bit 1):
  Parity bit for write data to be sent to disk -- to DPU (210-7421-A)

K50-K57:
  Write data to be sent to disk -- to DPU (210-7421-A)

OBS (Output Bus Strobe):
  Strobes write data from CPU's to disk -- from Port Expanders (210-7718)

OD1-OD4 (Output Data):
  Write data to be sent to disk -- from CPU's (22C80)

ODS (Output Data Strobe):
  Strobes write data from CPU's to disk -- from CPU's (22C80)

P1-P3 (Port):
  Select appropriate CPU port circuitry -- internal

RB (Ready/Busy):
  Disk ready/busy status -- from DPU (210-7421-A)
REQ1-REQ3 (Request):

Request by CPU for disk use -- from CPU's (22C80)

RESET1-RESET3:

Reset DPU and disk -- from CPU's (22C80)

RQ1_{1-3} (Request):

Request by CPU for disk use -- internal

RQ2_{41-4} (Request):

Request by CPU for disk use -- from Port Expanders (210-7718)

S0-S1 (Select):

Decoded into port select signals -- internal

STR (Strobe):

Strobes read data from disk to CPU's -- to Port Expanders (210-7718)
FIGURE 5 WL. NO. 210-7717 MULTIPLEXER BLOCK DIAGRAM