WANG LABORATORIES. INC.

MEMORANDUM

TO: 2200 Committee

FROM: Bob Kolk

DATE: June 22, 1972, Revised June 27, 1972

SUBJECT: 2200 I/O Specification

This memorandum contains a revision to the 2200
I/O Specifications and replaces the memorandum entitled
"I/O Specifications" dated March 13, 1972.

The major revisions to the 2200 I/O structure
include:

.   The Available connector signals have been
    made similar to the 700/600/500/400 I/O
    connector.

.   All 2200 devices including the keyboard and
    CRT are selectable by a 5-bit address setup
    in 5 IOB flip-flops from the KH and KL
    registers by a CIO command. The three IOB
    bits for the selection of 700C devices are
    available for their selection.

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I.   I/O Connector

Pins (1 - 8) $\overline{GKA}_0$ To $\overline{GKB}_3$

These are the input data lines for all devices. A device
must be enabled before Input data can be tansferred to the
CPU. (A device is enabled when an output strobe is made on
Pin 14 or Pin 31 with Pins (15 - 19) and (28 - 30) set to
the appropriate device address). If the device is a serial
device, the data must be transferred to Pin 5. The
information from these lines will be strobed into the 2200
KH and KL registers by the $\overline{GSIN}$ strobe on Pin 9. If the
KBD bit sensed on Pin 32, $\overline{GKBD}$, is set to a 1, the input
strobe will be inhibited by both the CPU, and the device.

Pin (9) $\overline{GISN}$

This is the input strobe signal to tell the CPU that the
data has been placed on the input data lines. The strobe
must be at least five micro-seconds. It will cause data
on Pins (1 - 8) to read into the 2200 KH and KL registers,
and will cause the keyboard/device ready-busy bit, KBD, to
be set in status Reg 1. If KBD is already set to 1, the
input strobe will be inhibited by the CPU, and the device.

Pin (10) $\overline{PRMS}$

This is an input/output Prime strobe which will be strobed
bi-directionally either as an output strobe from the CPU or
and input strobe from the keyboard. It will be a 5 micro-
second strobe initiated by the prime buttons on either the
CPU or keyboard. It will cause the CPU to enter the prime
micro-program routine, and will indicate this to outside
devices. (A second CPU trap location will be entered when
the CPU is powered on for master initialization)

Pin (11) $\overline{KFN}$

This signal indicates a Special Function Key has been depressed
on the keyboard, If a 1 is strobed into $ST1_2$ along with the
8-bit function code which is strobed in KH, KL. For other
devices the signal will not be connected and 0's will always
be strobed.

Pin (12) $\overline{RB}$

This is a input Ready/Busy D.C. level. A level on this pin is
returned to the CPU when an I/O device is enabled, to indicate
the device is available. This signal is read as a 1 in the low
order bit of status register 3, RB, when the device is present
and enabled. For all output devices the level will indicate
Ready/Busy after an I/O operation. (1 = Ready). The Ready/Busy
signal will be available 5 micro-seconds after a device is
enabled or strobed with output data.

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Pin (13) $\overline{HALT}$

This is a signal which is strobed into the CPU when the Halt button is depressed on the keyboard. It will cause bit 2 of status register 3, HALT, to be set to a 1.

Pin (14) $\overline{GISOE}$

This pin is used for a 5 micro-second device enable output strobe. This strobe along with the device address on Pins (15 - 19) causes most 2200 devices to be enabled. It is produced by a CIO instruction with bit 6 set equal to 1.

Pin (15 - 19) I_oB_o5 to I_oB_o1

These are device selection bits which contain the device address for 2200 peripherals other than the 700C devices. The pins reflect the contents of 5 IoB device address flops in the CPU. The flops are set from the contents the KL and the lower order bit of KH registers in the 2200 when a CIO command is executed with bit 7 set to 1. In addition, a device enable output strobe on Pin 14, $\overline{GISOE}$ is caused by the CIO with bit 6 set to a 1. A device senses this strobe along with the address in the IoB bits to become enabled. The device will become disabled at any point thereafter, when a susequent $\overline{GISOE}$ output strobe is made with any other address setup at Pins (15 - 19). 2200 device addresses should be switchable.

NOTE: Pins 28 thru 30, $\overline{IoB_1}$ to $\overline{IoB_3}$ are reserved for the selection of 700C type devices. These IoB flops are set from the high order 3-bits of KH when the CIO '1XX' is executed. They should be set to zeros when 2200 devices are enabled.

Pins (20 - 27) $\overline{GI_oB_oF_6}$ to $\overline{GI_oA_3F_6}$

These are output data lines from the CPU to outside devices. The information to be output is setup in the KH and KL registers of the CPU. It is transmitted to a device when an output strobe is made on Pin 31, $\overline{GISO}$, (By executing a CIO instruction with bit 5 set to a 1). When serial data is transmitted, Pin 27, $\overline{GI_oA_3F_6}$ should contain the serial data bit.

Pins (28 - 30) $\overline{I_oB_1}$ to $\overline{I_oB_3}$

These pins are used for the device selection address of 700C type devices. They reflect the contents of three IOB flip-flops reserved for this purpose. The flip-flops are set in the CPU from the high order three bits of the KH register, when a CIO instruction

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is executed with bit 7 set to one. When used with 700C devices, the address on these pins is generally strobed out by an output strobe signal on Pin 31, $\overline{GISO}$. (See 700 connector specifications for further details).

NOTE: When 700C devices are enabled, the 2200 device selection bits should be set to zero. The 2200 device selection bits are set from KL, and the low order bit of KH when a CIO instruction with bit 7 = to 1. These bits should be zero when setting up a 700C address.

Pin (31) $\overline{GISO}$

This pin is a five micro-second output strobe which is used to enable 700C devices and output data to devices. It is actuated in the CPU by executing a CIO instruction with bit 5 of the instruction set to a 1.

Pin (32) $\overline{GKBD}$

The pin is a D.C. level which reflects the status of the keyboard/device Ready/Busy bit, KBD, (Bit 1 of status register 1 in the CPU). The signal is used to enable or lockout the 'keyboard, and when doing I/O device processing to inhibit or allow input data strobes from the device. The KBD bit is set to 1 to lockout inputs, and set to a 0 to allows them.

Pins (33 - 36)   Common and Ground

Pin

33	IOV	Common
34	IOV	Common
35	IOV	Common
36	Chassis	Ground

NAME	PIN NO.	REMARKS
		INPUTS FROM EXTERNAL DEVICE
$\overline{GKA_0}$	1*	BCD 1
$\overline{GKA_1}$	2*	2 — High Order Code
$\overline{GKA_2}$	3*	4
$\overline{GKA_3}$	4*	8
$\overline{GKB_0}$	5*	BCD 1
$\overline{GKB_1}$	6*	2 — Low Order Code
$\overline{GKB_2}$	7*	4
$\overline{GKB_3}$	8*	8
$\overline{GISN}$	9*	Input Strobe from External Device
$\overline{PRMS}$	10*	Prime Output
$\overline{KFN}$	11*	Keyboard Special Function Input
$\overline{RB}$	12*	Ready/Busy (D.C. level)
$\overline{HALT}$	13*	Keyboard Halt
$\overline{GISOE}$	14*	Device Enable Output Strobe
$\overline{IoBo}_5$	15*	
$\overline{IoBo}_4$	16*	
$\overline{IoBo}_3$	17*	Device Address Selection Bits
$\overline{IoBo}_2$	18*	
$\overline{IoBo}_1$	19*	

NAME	PIN NO.	REMARKS
		GENERAL OUTPUTS
$\overline{GI_0 B_0 F_b}$	20*	BCD 1
$\overline{GI_0 B_1 F_b}$	21*	2 — Low Order Code
$\overline{GI_0 B_2 F_b}$	22*	4
$\overline{GI_0 B_3 F_b}$	23*	8
$\overline{GI_0 A_0 F_b}$	24*	BCD 1
$\overline{GI_0 A_1 F_b}$	25*	2 — High Order Code
$\overline{GI_0 A_2 F_b}$	26*	4
$\overline{GI_0 A_3 F_b}$	27*	8
$\overline{I_0 B_1}$	28*	I/O Bus & Group I & II Code
$\overline{I_0 B_2}$	29*	
$\overline{I_0 B_3}$	30*	
$\overline{GISO}$	31*	Output Data Strobe
$\overline{GKBD}$	32*	Keyboard Condition Indicator
±OV	33*	Common
±OV	34*	Common
±OV	35*	Common
Chassis Ground	36*	Chassis Ground
	37*	+17 V
	38*	-17 V
	39*	Key
	40*	
	41*	+5V
	42*	-5V
	43*	24 VAC
	44*	24 VAC

* All 2200 Devices including the keyboard and CRT are interfaced to the 2200 via control cards. Therefore pin assignment listed above are variable.

II - I/O Connector (As seen by the micro-program)

The status registers (ST1 - ST4), the KH and KL registers, the CIO
instruction and micro-program location 0 are all used for I/O
processing and effect the I/O connector as follows:

ST1 - Status Register 1

3	2	1	0
Mem	KFN	KBD	Ca

Carry
Used internally in CPU for add, subtract, etc.
(0 = no carry, 1 = carry)   (M/H)

I/O Ready/Inhibit   (M/H)

KBD = 0   Allow input from keyboard or selected
I/O device
KBD = 1   Inhibit inputs from keyboard or selected
device

When a device or the keyboard strobe into the CPU,
KBD will be set to 1.

Keyboard Special Function Input (= 1 when the input
just received from the keyboard is a special
Function Code)   (M/H)

RAM/ROM 8-bit memory selection
Used internally in CPU only.
(0 = RAM, 1 = ROM)   (M)

Note: (M) = Set by micro-program only
(H) = Set by hardware only (D.C. level)
(M/H) = Set by both micro-program and hardware. (Strobe)

ST2 - Status Register 2

```
    3   2   1   0
  ┌───┬───┬───┬───┐
  │   │   │   │   │
  └───┴───┴───┴───┘
   _____/
```
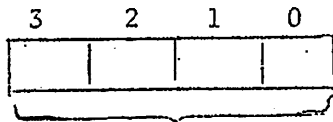
Spares used by micro-program for internal use.   (M)

ST3 - Status Register 3

```
    3     2     1    0
  ┌─────┬─────┬─────┬─────┐
  │ ADM │HALT │ DE  │ RB  │
  └─────┴─────┴─────┴─────┘
     ↑     ↑     ↑     ↑
```

Device Enabled, Ready/Busy   (H)
(D.C. level)
RB = 1   Device Enabled or (Ready)
RB = 0   Device Not Enabled or (Busy)

Decimal Add/Subtract Error Bit   (M/H)

Keyboard Halt (single step key)   (M/H)
STEP = 0   No Halt or Interrupt
STEP = 1   Halt/Interrupt

8-Bit Addressing Mode (M)
(Internal CPU use only)
ADM = 0   Vertical Mode $\pm$ 16
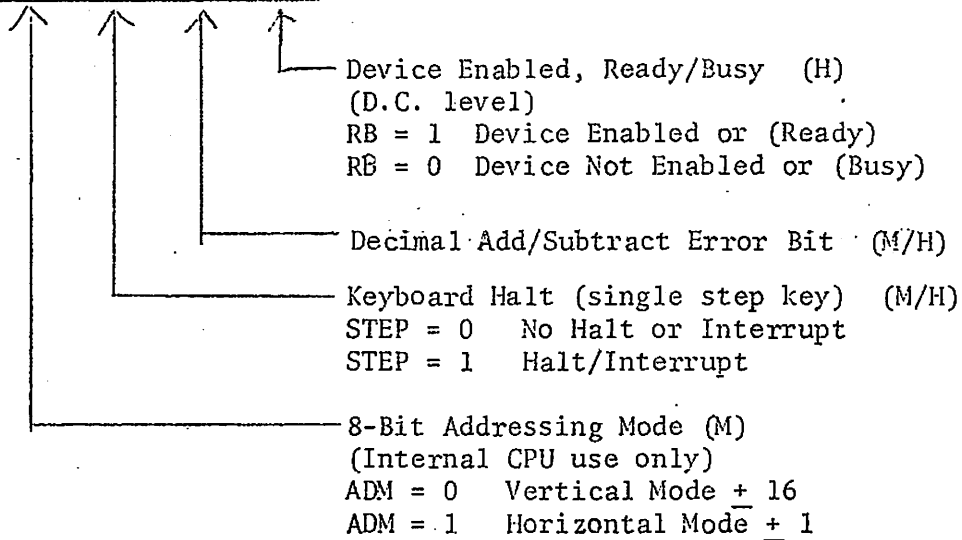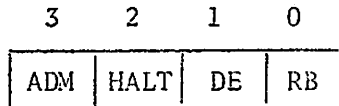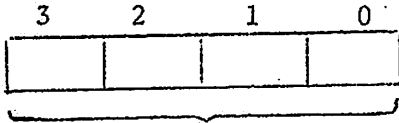ADM = 1   Horizontal Mode $\pm$ 1

Note: (M)   = Set by micro-program only
        (H)   = Set by hardware only (D.C. level)
        (M/H) = Set by micro-program or hardware (Strobe)
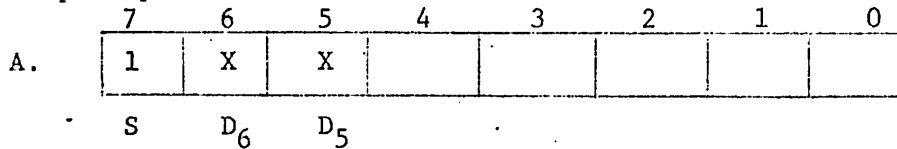
ST4 - Status Register 4

```
   3      2      1      0
 ┌──────┬──────┬──────┬──────┐
 │      │      │      │      │
 └──────┴──────┴──────┴──────┘
 └────────────────────────┘
```

Spares available for Internal CPU use   (M)

CIO Instruction

The CIO operand SD_6D_5 directly effects the I/O connector: Any or all of these three bits may be set to 1 to cause output strobes and set the device address flip-flops

A.

7	6	5	4	3	2	1	0
1	X	X					

S D_6 D_5

When a CIO instruction is executed with S = 1:

- The 4-bits in the KL register and the low order bit of KH register are used to set the IoB address flops associated with Pins 15 - 19 of the I/O connector.

$$KL_0 \rightarrow IoBo_1 \quad Pin\ (19)$$
$$KL_1 \rightarrow IoBo_2 \quad Pin\ (18)$$
$$KL_2 \rightarrow IoBo_3 \quad Pin\ (17)$$
$$KL_3 \rightarrow IoBo_4 \quad Pin\ (16)$$
$$KH_0 \rightarrow IoBo_5 \quad Pin\ (15)$$

- The high order 3-bits of the KH register are used to set the 700C device IoB flops, Pins 28 - 30.

$$KH_1 \rightarrow IoBo_1 \quad Pin\ (28)$$
$$KH_2 \rightarrow IoBo_2 \quad Pin\ (29)$$
$$KH_3 \rightarrow IoBo_3 \quad Pin\ (30)$$

B.

7	6	5	4	3	2	1	0
X	1	X					

S D_6 D_5
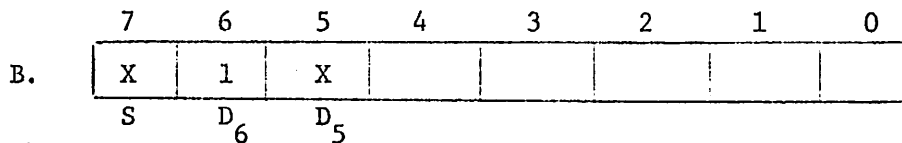
When a CIO instruction is executed with the D_6 bit = 1:

- A 5 micro-second output strobe is generated on Pin 14, $\overline{GISOE}$. This strobe is generally used to enable and disable 2200 devices other than the 700C device. The strobe is generally used conjunction with the Address set up in $IoBo_1$ to $IoBo_5$, Pins 19 to 15.

7	6	5	4	3	2	1	0
X	X	1					

S D_6 D_5
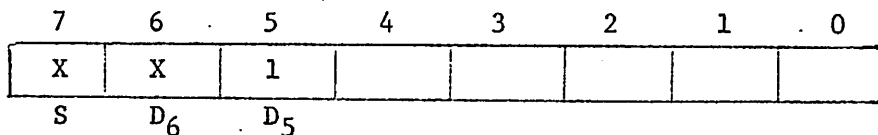
When a CIO instruction is executed with the D_5 bit set = 1:

- A 5 micro-second strobe is generated on $\overline{GISO}$, Pin 31. This strobe is generally used to send data from the KH and KL registers out to an output device via Pins 20 to 27. In addition, for 700C devices, the strobe is used to enable and control these devices via the setting of the 700C IoB flops, Pins 28 to 30.

Prime Input/Output

A prime button is available on both the CPU and the keyboard. When it is depressed from either position, a Bi-directional strobe is generated on Pin 10 of the connector which cause the CPU to automatically start executing at address 0000.   The 5 micro-second strobe will also cause certain devices to initialized. (A trap to location 1 is triggered when the CPU is turned on for master initialization).

Relationship Between CPU registers, and I/O connector

The following table summarizes the relationship between the 2200 CPU I/O associated registers and commands and the I/O connector.

Pin

1	$\overline{GKA_0} \rightarrow KH_0$	Data Input from Keyboard or I/O Device
2	$\overline{GKA_1} \rightarrow KH_1$	
3	$\overline{GKA_2} \rightarrow KH_2$	
4	$\overline{GKA_3} \rightarrow KH_3$	
5	$\overline{GKB_0} \rightarrow KL_0$	
6	$\overline{GKB_1} \rightarrow KL_1$	
7	$\overline{GKB_2} \rightarrow KL_2$	
8	$\overline{GKB_3} \rightarrow KL_3$	
9	$\overline{GISN} \rightarrow ST1_1$	Input Data Strobe
10	$\overline{GPMS}$ 0000 $\rightarrow IC_1$ to IC_4,	Prime Signal for CPU, I/O Devices
11	$\overline{KFN} \rightarrow ST1_2$	Keyboard Special Function Input
12	$\overline{RB} \rightarrow ST3_0$	Device Enabled/Ready D.C. level (1 = Enabled/Ready)
13	$\overline{HALT} \rightarrow ST3_2$	Halt/Step Strobe (1 = Halt/Step Depressed)
14	$\overline{GISOE}$ Output Strobe when CIO 'X1X'	Used to enable/disable 2200 devices
15	$KL_0 \rightarrow IoBo_1$ flop	2200 Device Address, Set when CIO '1XX' instruction
16	$KL_1 \rightarrow IoBo_2$ "	
17	$KL_2 \rightarrow IoBo_3$ "	
18	$KL_3 \rightarrow IoBo_4$ "	
19	$KH_0 \rightarrow IoBo_4$ "	
20	$KL_0 \rightarrow \overline{GIoBoF}$	Data Output from CPU to Device, (when CIO 'XX1')
21	$KL_1 \rightarrow \overline{GIoB_1F}$	
22	$KL_2 \rightarrow \overline{GIoB_2F}$	
23	$KL_3 \rightarrow \overline{GIoB_3F}$	
24	$KH_0 \rightarrow \overline{GIoAoF}$	
25	$KH_1 \rightarrow \overline{GIoA_1F}$	
26	$KH_2 \rightarrow \overline{GIoA_2F}$	
27	$KH_3 \rightarrow \overline{GIoA_3F}$	
28	$KH_1 \rightarrow IoB_1$ flop	700C Device Address, Set when CIO '1XX' instruction
29	$KH_2 \rightarrow IoB_2$ flop	
30	$KH_3 \rightarrow IoB_3$ flop	
31	$\overline{GISO}$ Output Strobe for Data Output, 700C Device Enable, when CIO 'XX1'	
32	$ST1_1 \rightarrow \overline{GKED}$ Inhibit/Enable I/O device input. (Inhibit when $ST1_1$,(KBD) = 1)	

III. Typical I/O Sequences

A. CRT (Output Only), (Teletype Output also identical)

    i. Hardware

The CRT is enabled by a Device Enable output strobe on Pin 14, with Pins 15 thru 19 set to the CRT device address (00010). It is disabled by an output strobe on Pin 14 with Pins 15 thru 19 set to any other device address. The CRT accepts 8-bits of parallel data from Pins 20 thru 27 when a data output strobe is available on Pin 31. When the CRT has accepted the data and is ready for another output, it will indicate ready by D.C. level on Pin 12 , $\overline{RB}$, (1 = Ready; i.e. $\overline{RB}$ = 0) The 2200 may upon occasion output upper and lower case ASCII code. To make this display properly on the CRT, the CRT must transpose codes 110XXXX and 111XXXX to 100XXXX and 101XXXX.

    ii. Micro-program

Data is output to the CRT in ASCII code by the following sequence:

(1) Inhibit Keyboard or other input strobes by setting KBD = 1 for at least 10 micro-seconds prior to enable strobe

(2) Enable the CRT:
    . Set up Device Address 0000 → KH
                               0010 → KL
    . Set flops and strobe CIO '11000000'

(3) Delay 5 micro-seconds and check for Enabled and Ready, $(ST3_0$, (RB), =1)

(4) Set up next character in KH, KL

(5) Strobe out data (CIO '00100000')

(6) Delay 5 micro-seconds and wait for Ready from CRT, i.e. $(ST3_0$ (RB) = 1)

(7) Repeat (3) thru (5) for all characters

(8) Disable CRT:
    . Set up zero Device Address 0000 → KH, KL
    . Set flops and strobe CIO '11000000'

B. · Keyboard (Input Only) (Teletype input also identical)

    i.   Hardware

The keyboard is enabled by an Device Enable output strobe on Pin 14, with Pins 15 thru 19 containing a device address of (00001). It is disabled by a similar strobe with the device address set to any other value.

When a keyboard key is depressed, an input strobe is generated on Pin 9 and 8-bits of parallel data are strobed in via Pins 1 thru 8 into the KH and KL registers. Since the input strobe set $ST1_1$ (KBD), the keyboard will be locked out again until KBD is reset.

When the prime button on the keyboard is depressed, a 5 micro-second strobe will be generated on Pin 10.

When the Halt/Step key on the keyboard is depressed, a 5 micro-second strobe will be generated on Pin 13. This will cause bit 2 of ST3 to be set to a 1.

When a special function key is depressed, a signal on Pin 11, $\overline{KFN}$ will set bit 2 of status register 1 to a 1, in addition to the normal 8-bit KH, KL input.

  ii.   Micro-program

ASCII data is input from the keyboard by the following sequence:

    (1)   Inhibit other input strobe by setting KBD = 1 for at least 10 micro-second prior to enabling the keyboard.

    (2)   Enable the Keyboard
        . Set up Device Address 0000 → KH
                                 0001 → KL
        . Set flops and strobe CIO '11000000'

    (3)   Delay 5 micro-seconds, then check keyboard Enabled ($ST3_0$ (RB) = 1)

    (4)   Enable for input 0 → $ST1_1$ (KBD)

    (5)   Wait for Input Ready ($ST1_1$ (KBD) = 1)

    (6)   Process character received in KH, KL. Repeat 4 and 5 for additional characters or leave the keyboard locked (i.e. KBD = 1) for CPU processing.

    (7)   When doing I/O processing with other devices the keyboard is locked by setting up a different device address and strobing $\overline{GISOE}$. i.e. . Device Address → KH, KL
               . CIO '11000000'

C.   Cassette Magnetic Tape (General)

   i.   General Discussion of Cassette Operation

        A 400/500/600 type single track cassette will be used
        for the 2200 console cassette tape.

        Figure 2 illustrates the recording current, flux change
        and playback signals associated with the 2200 cassette
        format.

        A record on cassette tape consists of one or more words
        of 4-bits each of which followed by an odd parity bit.
        Higher priority bits are always recorded 1st. The record
        is preceeded and followed by a record gap equivalent to
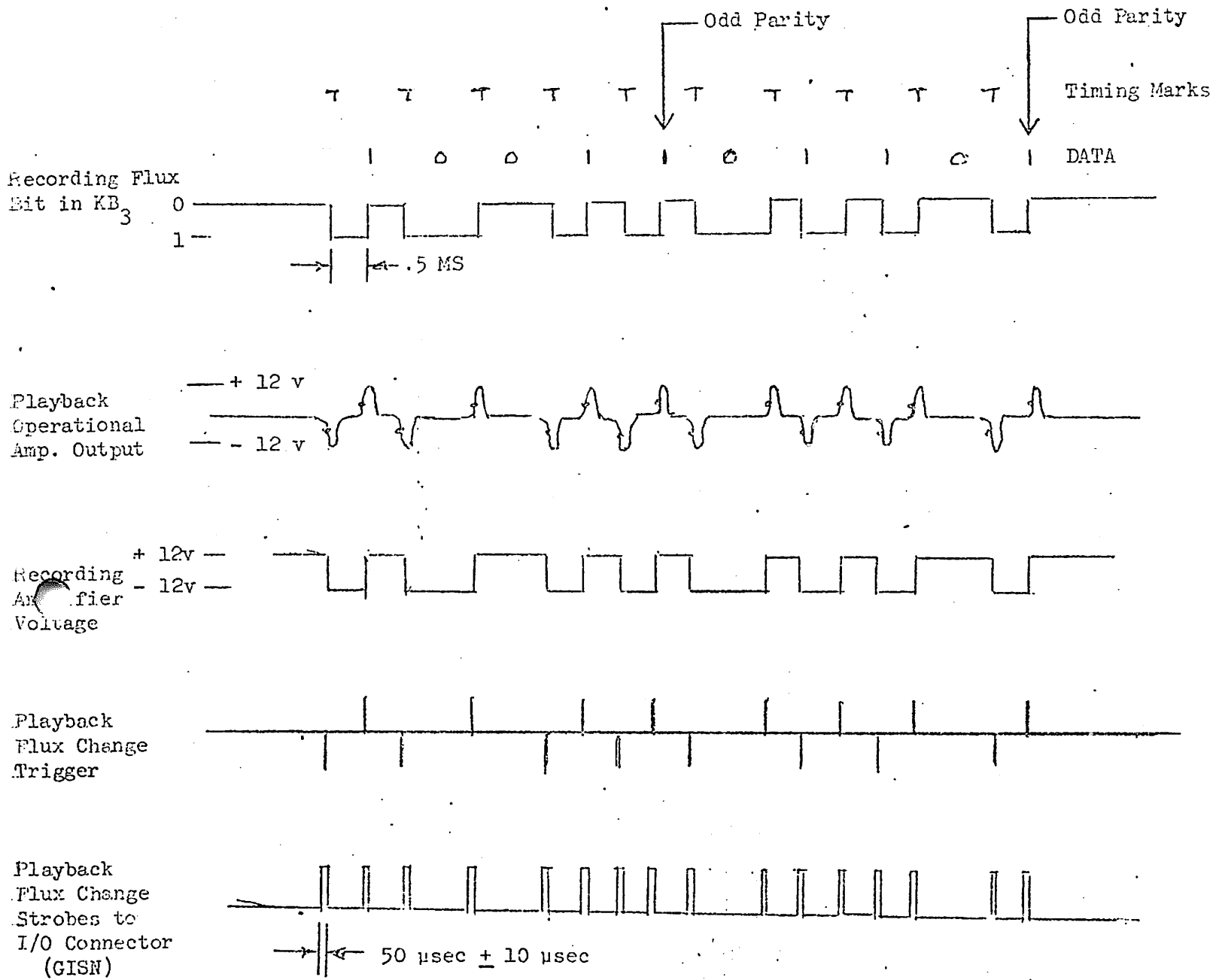   the stop and start time of the cassette.

        For a single track cassette such as the 2200, the recording
        current is varied between two values which produce a peak
        recording voltage of either + or - 12 volts at the head.
        This produces areas on the tape which are magnetized in
        either a forward or reverse polarity. Because of the large
        variation in tolerences of the tape, however, data is
        represented by changes in flux within certain time cycles.

        Interrecord Gap is written by a constant recording current
        (and flux). Each bit on a record is preceeded by a
        timing mark, which is a reversal in recording current
        (and flux). After each timing mark a one is recorded if the
        recording current (and flux) is reversed after .5 MS of tape
        motion. If there is no reversal in recording current
        (and flux) until the next timing mark (1.0 MS later), the
        bit is a zero. Upon playback the read head electronics
        sense changes in flux and strobes them into the micro-
        processor. To allow for skew in the tape, the micro-program
        can set a time window to look for a flux change after each
        timing mark flux change. (From Timing Mark + 150 µs to
        timing mark to 700 µs) or a variation of approxiately 50%.
        There after the next timing mark is picked up and next data
        bit (flux change or no flux change) is synchronized on it.

        In the example in Figure 2 two 4-bit words (1001) and (0110)
        are recorded on tape. Since an odd parity bit follows each
        4-bits the total record image becomes (1001101101).

Figure 2   2200 CASSETTE FORMAT, RECORDING AND PLAYBACK SIGNALS

EXAMPLE: Recording and Playback of two four bit words, (1001) and (0110).

Odd Parity

Odd Parity

Timing Marks

T T T T T T T T T T

1 0 0 1 1 0 1 1 0 1   DATA

Recording Flux
Bit in KB_3   0
               1

|← .5 MS

Playback
Operational
Amp. Output

+ 12 v

− 12 v

Recording
Amplifier
Voltage

+ 12v
− 12v

Playback
Flux Change
Trigger

Playback
Flux Change
Strobes to
I/O Connector
(GISN)

← 50 μsec ± 10 μsec

- Look for timing mark flux change, T
- After T found, look for data flux change between T + 150 μsec T + 700 μsec.
- After T + 700 μsec, look for next timing mark, etc.
- If no timing mark for 2 MS, end of record.
- If last bit in record not parity bit, and if not at least one word read assume noise and start again.

ii. Hardware

(1) The cassette tape is enabled by an output strobe on Pin 31, with Pins 15 thru 19 set to the cassette address (00011). It is disabled by a Pin 31 output strobe with Pins 15 thru 19 set to any other address. (Note - the Pin 31 output strobe is used for the enabling/disabling strobe instead of the Pin 11 strobe, because the cassette unit is being designed to be compatible with both the 400 and 2200). When the cassette is disabled by a new device address or by a prime strobe on Pin 10, the cassette should return to null conditions of recording current off and motor off.

(2) Motor ON/Motor OFF will be controlled by signal sent via an output strobe on Pin 31 equivalent to 1 or 0 bit in the KH register bit 0. On the I/O connector this is sensed by $GIoAoF$ (Pin 24) where:

$$\text{Motor OFF} \ - \ KHo = 0 \qquad \overline{GIoAoF} = 1$$
$$\text{Motor ON} \ - \ KHo = 1 \qquad \overline{GIoAoF} = 0$$

(3) Recording Current ON/OFF will be controlled by a signal sent by a output strobe on Pin 31 equivalent to a 1 or 0 in the KH register bit 1. On the I/O connector this is sensed at $GIoA1F$ (Pin 25).

$$\text{Recording Current ON} \ - \ KH1 = 1 \ \ \overline{GI_0A_1F} \ (\text{Pin 25}) = 0$$
$$\text{Recording Current OFF} \ - \ KH1 = 0 \ \ \overline{GI_0A_1F} \ (\text{Pin 25}) = 1$$

(4) Recording Flux Bit will be sent via an output strobe on Pin 31. It is stored in the high order bit of the KL register (KL_3). On the I/O connector this is $\overline{GIoB_3F}$, Pin 23. When the recording current bit is on, ($KH_1 = 1$), the D.C. level will be used to hold the recording voltage to $\pm$ 12 volts at the recording amplifier.

$$KL_3 = 1 \ , \quad \overline{GIoB_3F} = 0 \quad (- 12 \text{ volts})$$
$$KL_3 = 0 \ , \quad \overline{GIoB_3F} = 1 \quad (+ 12 \text{ volts})$$

When writing Gaps this bit should be set to + 12 volts ($KL_3 = 0$). Since each 4-bits written will always be followed by an odd parity bit, the recording voltage will always return to + 12 volts at each interrecord gap.

(5) Playback Flux Change will be sensed by a bit strobed into the low order bit of KL (KL_0). A flux change strobe will occur if the recording current bit is OFF ($\overline{GI_0A_1F}$, Pin 25 = 1) every time the cassette read logic senses a flux change during playback. A 1-bit will then be strobed in KL_0 via $\overline{GKB_0}$, Pin 5. In addition KBD will be set to 1 via the input strobe, $\overline{GISN}$, Pin 9. If KBD, (Pin 32) is set to 1, the input strobe will be inhibited.

(6) When enabled, the cassette will return a D.C. level on Pin 12, (Ready/Busy). This will be sensed as a 1 in the low order bit of status register 3 by the micro-program to determine whether the cassette is operative.

Figures 3 and 4 illustrate the 2200 register bits and I/O connector signals used for cassette operations.
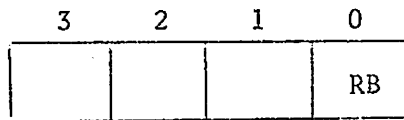
Figure 3   2200 REGISTER BITS USED FOR CASSETTE OPERATION
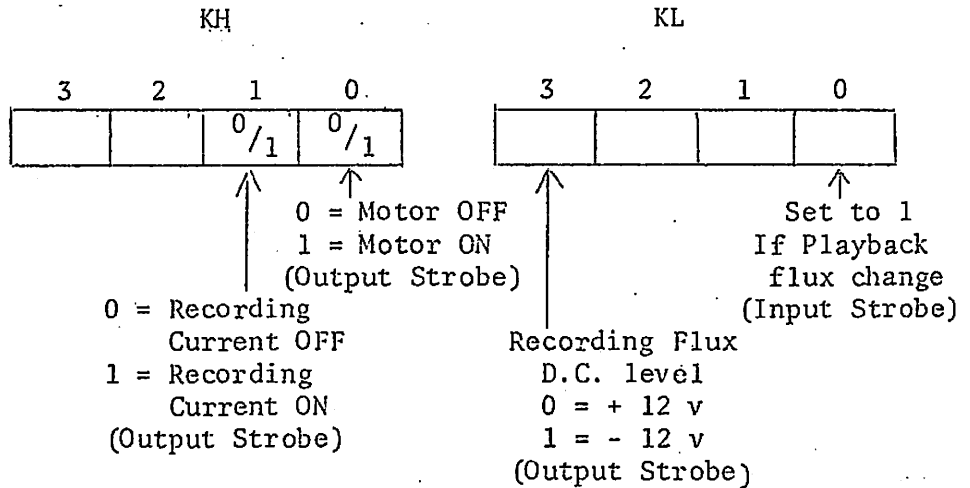
ST1 - Status Register 1

3	2	1	0
		KBD	
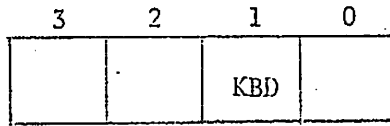
When set = 0 Input flux change
            strobes can occur.
set = 1 When an input flux
        strobe occurs.

ST3 - Status Register 3

3	2	1	0
			RB

D.C. level Ready/Busy
set to 1 when cassette
enabled.

KH and KL Registers

KH

3	2	1	0
		$^0/_1$	$^0/_1$

KL

3	2	1	0

0 = Motor OFF
1 = Motor ON
(Output Strobe)

0 = Recording
    Current OFF
1 = Recording
    Current ON
(Output Strobe)

Set to 1
If Playback
flux change
(Input Strobe)

Recording Flux
D.C. level
0 = + 12 v
1 = - 12 v
(Output Strobe)

In addition KH and KL are used to set up the device address

Figure 4   2200 I/O CONNECTOR SIGNAL FOR CASSETTE OPERATION

NAME	PIN NO.	DESCRIPTION
$\overline{GKB}_0$	5	Playback flux change input.
$\overline{GISN}$	9	Input strobe when playback flux change.
$\overline{RB}$	12	Ready/Busy D.C. level.
$\overline{IoBo}_1$	15	Device Address for enable '00011'
$\overline{IoBo}_2$	16	
$\overline{IoBo}_3$	17	
$\overline{IoBo}_4$	18	
$\overline{IoBo}_5$	19	
$\overline{GIoB_3F}$	23	Recording flux D.C. level (0 = -12v, 1 = +12v)
$\overline{GIoAoF}$	24	Motor ON/OFF
$\overline{GIoA_1F}$	25	Recording Current ON/OFF
$\overline{GKBD}$	32	Keyboard Condition Indication (Input strobes inhibited if KBD = 1)

iii Micro-program For Cassette Recording

(1) Inhibit keyboard or other input strobes by setting
     KBD = 1 for at least 10 micro-seconds prior to enabling
     the cassette

(2) Set up Device Address in Flops
     . Address into KH, KL - $0000 \rightarrow$ KH $0011 \rightarrow$ KL
     . Set flops   -   CIO '10000000'

(3) Set up Motor ON and Recording Current ON bits
           $(0011 \rightarrow$ KH)

(4) Set up +12 volt flux level $(0000 \rightarrow$ KL)

(5) Strobe to Enable Cassette and Set Motor, Current
     and Flux Bits.   CIO   '01100000'

(6) Wait for 5 micro-seconds and check if Cassette Enabled
           $(ST3_0$, RB = 1)

(7) Delay for 1/2 second. This writes an interrecord gap
     and allows the cassette to get up to speed.

(8) Complement the Bit in KL_3 and strobe it out
     (CIO '00100000') to produce the 1st timing mark.
     If the first bit to be output is a 1, delay .5 MS,
     then complement KL_3 and strobe it and wait .5 MS
     and put out another timing mark. If the 1st bit
     is 0, delay a full 1 MS complement KL_3 and strobe it
     to produce the next timing mark. Repeat this process
     for all Marks, data bits, and parity bits to be
     recorded. (See Figure 2). (A timing mark flux change
     occurs every 1 MS. If a one bit is to be output a
     flux change occurs at .5 MS between the two marks, if
     a 0 bit none occurs).

(9) At the end of the record, leave KL_3 set to the last
     setting (0), turn the Motor OFF but leave the
     recording current ON, (i.e. $0010 \rightarrow$ KH) and strobe
     CIO '001000000'. (leave KBD set to 1 to inhibit input
     strobes)

(10) Delay for 1/2 second to allow the tape motion to stop.

(11) Disable the cassette
           . $0000 \rightarrow$ KH, KL
           . Set flops CIO '10100000'

iiii. Micro-program For Cassette Playback

(1) Inhibit the keyboard and other input strobes by setting KBD = 1 at least 10 micro-seconds prior to enabling the cassette

(2) Set up Device Address in I B flops
. Address into KH, KL 0000 → KH 0011 → KL
. Set flops CIO '10000000'

(3) Set up Motor ON, Recording Current OFF Bits
(0001 → KH) (0000 → KL)

(4) Strobe to Enable Cassette and set up Motor, Current bits CIO '00100000'

(5) Delay 1/6 seconds

(6) Reset KL and KBD bits to receive flux
(0000 → KL, 0 → KBD)

(7) Wait for timing flux change strobe
(i.e. KBD = 1, KL = 0001)

(8) When timing flux change received, delay 150 μsec and then reset KL and KBD to receive a data flux change. (0000 → KL, 0 → KBD)

(9) Delay for 550 μsec waiting for data flux change. (i.e. 1 → KL, 1 → KBD). If not received assume a 0 bit and go back to wait for next timing assume a 1 bit change. If flux change received within 550 μsec, delay rest of that period, then reset KL and KBD and wait for the next timing flux change. (i.e. repeat 6 thru 9)

(10) Check each fifth bit for odd parity and then store the 4-bit word.

(11) If no timing bit is received for 2 MS, then assume end of record gap. If the gap is sensed but the number of bits received not a multiple of 5, (i.e. last bit received not a parity bit), and at least one good 4-bit word and parity has not been read, then reset memory address back to starting address, assume noise has been received and start again.

(12) When an entire record has been received, (with or without correct parity) turn the motor OFF and delay 1/2 second
. Set up Motor OFF Bit 0000 → KL
. Strobe CIO '00100000'

(13) Disable Cassette
- Set up zero address 0000 → KH, KL

- Strobe to Cassette CIO '10100000'

MEMORANDUM

TO: R. Kolk
FROM: B. Patterson
DATE: November 21, 1973
SUBJECT: 2200 I/O Microprogramming Notes

Certain aspects of I/O microprogramming for the 2200 are not obvious from the present literature. Hopefully, this memo will eliminate some of the confusion.

2200 I/O STROBES

1.   ABS, Address Bus Strobe (580C0)

     Each 2200 device has a unique 8-bit device address associated with it. Only one device may be enabled (active) at a time. A device is enabled if its device address is loaded into the IOB address flip-flops. The ABS transfers the device address specified by the registers KH and KL into the IOB's. KH and KL may not be modified for 5 μsec following the strobe.

     Example: MVI 1, KH   device address = 1A
                           MVI A, KL
                           CIO '11000000' ABS strobe
                           SB DELAY 5   delay 5 μsec

2.   OBS, Output Bus Strobe (58020)

     OBS is a 5 μsec data output strobe that sends the data in the KH and KL registers out to the device which is currently enabled. KH and KL must not be modified for 5 sec following the strobe. Generally, the microprogram should check if the device is ready before the strobe is executed.

DEVICE READY/BUSY (ST3$_o$)

$ST3_o$ = 0 $\Rightarrow$ device busy
$ST3_o$ = 1 $\Rightarrow$ device ready

     Example: MV S3, F1
                           BF 1, F1, *-1   wait until device ready
                           CIO '00100000'   strobe data
                           SB DELAY 5   delay 5 μsec

3. IBS, Input Bus Strobe

IBS is a 5 μsec data input strobe that transfers 8-bits of data from the input device into the KH and KL registers. The data is allowed to enter the CPU only if the device is enabled and if KBD (ST1$_2$) = 0. After the input strobe is received by the CPU, the hardware sets KBD = 1. KH and KL must not be modified for 5 μsec following the input strobe.

```
KBD, CPU READY/BUSY (ST1₂)

ST1₂ = 0 ──▶ CPU ready, allow input
ST1₂ = 1 ──▶ CPU busy, inhibit input
```

Example:

ANDI	D, S1, S1		allow input, KBD = 0
MV	S1, F1		
BF	2, S1, *-1		wait for input
SB	DELAY 5		delay 5 μsec.

4. CBS, Request Input Strobe (58010)

CBS is a 5 μsec output strobe that requests the currently enabled device to send in an IBS. For example, a CBS to the tape cassette drive causes the drive to strobe the current tape status into KH and KL. KBD must be set to 0 before the strobe in order to allow the IBS to come in; KBD is set to 1 by the hardware after the strobe. KH and KL may not be modified for 5 μsec following the strobe.

Example:

ANDI	D, S1, S1	KBD = 0, allow input
CIO	'00010000'	CBS strobe
SB	DELAY 5	delay 5 μsec
MV	S1, F1	make sure KBD = 1
BF	2, F1, *-1	

KBD, CPU READY/BUSY STATUS BIT (ST1₂)

KBD is used to allow (KBD = 0) or inhibit (KBD = 1) input strobes from entering the CPU. When KBD = 1, KH and KL can be used by the microprogram as general registers. When KBD = 0, KH and KL should only be modified by an input strobe. KBD should always be set equal to 1 unless the microprogram is awaiting an input strobe.

Modifying KBD:

After changing KBD from 0 to 1, KH and KL may not be used for 10 μsec
in order to insure that an IBS will not change KH and KL.

Example: ⟶

ORI 2, S1, S1   KBD = 1
SB   DELAY 10   delay 10 μsec.

Testing KBD:

In order to insure that KBD does not change while it is being tested
(this condition can cause an illegal branch in the microcode), status
register 1 should be moved to a file register and KBD tested in the
file register.

Example: ⟶

MV   S1, F1   move status to file reg.
BF   2, F1, *-1   test KBD

See the memo "2200 I/0 Specifications" dated June 22, Revised June 27
for further details on I/0.